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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,606	02/26/2002	Michael Karl Gschwind	YOR920020001US1	8683

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EXAMINER

MEONSKE, TONIA L

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/085,606

Applicant(s)

GSCHWIND ET AL.

Examiner

Tonia L Meonske

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>2/19/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 9, 11, 12, 14-19, 22, 24, 25, and 27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hum et al., US Patent 6,594,730.
4. Referring to claim 1, Hum et al. have taught in a processor, an apparatus for issuing instructions, comprising:
 - a. a classification logic adapted for prioritizing instructions in relation to one another and sorting said instructions in a number of priority categories (abstract, column 2, lines 12- 64, column 3, lines 13-51);
 - b. a plurality of instruction queues, wherein said plurality of said queues matches said number of said priority categories, and wherein each of said queues adapted to receive only one of said priority categories of said instructions from said classification logic, whereby said queues having same priority categories as said instructions (abstract,

column 2, lines 12- 64, column 3, lines 13-51, Figure 1, elements 145, 150, 160, 170, and 190); and

c. an issue logic operably coupled to said plurality of instruction queues and selecting from which of said queues to dispatch said instructions for execution, wherein said issue logic has been designed to be cognizant of said priority categories of said queues (abstract, column 2, lines 12- 64, column 3, lines 13-51, Figure 1, element 200).

5. Referring to claim 2, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus forms part of an in-order instruction issue processor architecture (column 2, lines 12-21).

6. Referring to claim 3, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus forms part of an out-of-order instruction issue processor architecture (column 2, lines 12-21).

7. Referring to claim 4, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said plurality of instruction queues consist of two queues, a high priority queue (Figure 1, elements 140, 150, 160, and 170) and a low priority queue (Figure 1, element 190).

8. Referring to claim 5, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said instructions sorted in said number of priority categories by said classification logic comprise cloned instructions (column 2, lines 12- 64, The prefetch instructions are cloned from future instructions to be executed in order to prefetch upcoming needed data into the cache.).

9. Referring to claim 6, Hum et al. have taught the apparatus for issuing instructions of claim 5, as described above, and wherein said cloned instructions and corresponding unmodified instructions from which said cloned instructions have been derived are found in different ones of said priority category queues (Figure 1, Regular instructions are stored in elements 140, 150, 160, and 170, and prefetch instructions, which have a lower priority, are stored in element 190).

10. Referring to claim 9, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said prioritizing of said instructions is based on a probability for memory miss (column 4, lines 12-50, column 5, lines 50-57).

11. Referring to claim 11, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus is designed for prioritizing and issuing said instructions in a dynamic manner (column 2, lines 12- 64, column 3, lines 13-51, The second arbiter, element 200, is adapted to dynamically disregard requests received from the prefetch queue when the queue is congested.).

12. Referring to claim 12, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus further comprising a predictor unit operably coupled to said classification logic, wherein said predictor unit identifies performance-critical instructions (column 2, lines 12- 64, A prefetch instruction is not a performance critical instructions and as such is identified as a lower priority instruction.).

13. Claim 14 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

14. Claim 15 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

15. Claim 16 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

16. Claim 17 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

17. Claim 18 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

18. Claim 19 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

19. Claim 22 does not recite limitations above the claimed invention set forth in claim 9 and is therefore rejected for the same reasons set forth in the rejection of claim 9 above.

20. Claim 24 does not recite limitations above the claimed invention set forth in claim 11 and is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

21. Claim 25 does not recite limitations above the claimed invention set forth in claim 12 and is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

22. Referring to claim 27, Hum et al. have taught a program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for issuing instructions as recited in claim 14 (Figure 1, element 210).

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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24. Claims 1, 10, 13, 14, 23, and 26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bain, Jr. et al., US Patent 4,829,425.

25. Referring to claim 1, Bain, Jr. et al. have taught in a processor, an apparatus for issuing instructions, comprising:

- a. a classification logic adapted for prioritizing instructions in relation to one another and sorting said instructions in a number of priority categories (column 15, lines 30-40, Low priority instructions are classified in the low priority queue and the high priority instructions are classified in the high priority queue.);
- b. a plurality of instruction queues, wherein said plurality of said queues matches said number of said priority categories, and wherein each of said queues adapted to receive only one of said priority categories of said instructions from said classification logic, whereby said queues having same priority categories as said instructions (column 15, lines 30-40, Low priority queue receives low priority instructions and the high priority queue receives high priority instructions.); and
- c. an issue logic operably coupled to said plurality of instruction queues and selecting from which of said queues to dispatch said instructions for execution, wherein said issue logic has been designed to be cognizant of said priority categories of said queues (column 15, lines 30-68).

26. Referring to claim 10, Bain, Jr. et al. have taught the apparatus for issuing instructions of claim 1, as described above, and wherein said apparatus is designed for prioritizing and issuing said instructions in a static manner (column 15, lines 30-40, The programmer provides a static channel number, either 14 or 15.).

27. Referring to claim 13, Bain Jr., et al. have taught the apparatus for issuing instructions of claim 1, wherein said classification logic further adapted for receiving preannotated instructions, wherein said instructions have been preannotated during compilation time and said preannotations indicate said priority categories (column 15, lines 30-40).

28. Claim 14 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

29. Claim 23 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

30. Claim 26 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

32. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bain, Jr. et al., US Patent 4,829,425, in view of Wulf et al., US Patent 6,154,826.

33. Referring to claim 7, Bain Jr. et al. have taught the apparatus for issuing instructions of claim 1, as described above. Bain Jr. et al. have not taught wherein said prioritizing of said instructions is based on said instructions being scalar instructions or vector instructions. Wulf et al. have taught wherein said prioritizing of said instructions is based on said instructions being scalar instructions or vector instructions (column 2, line 60-column 3, line 37) for the desirable

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purpose of avoiding memory bottlenecks. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the prioritizing of the instructions in Bain Jr. et al. based on said instructions being scalar instructions or vector instructions, as taught by Wulf et al., for the desirable purpose of avoiding memory bottlenecks (column 2, line 60-column 3, line 37).

34. Claim 20 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

35. Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hum et al., US Patent 6,594,730, in view of Taniani et al., US Patent 5,655,114.

Referring to claim 8, Hum et al. have taught the apparatus for issuing instructions of claim 1, as described above. Hum et al. have not specifically taught wherein said prioritizing of said instructions is based on a conditionality of branching. However, Taniani et al. have taught prioritizing of said instructions is based on a conditionality of branching (column 3, lines 46-52, column 11, line 35-column 12, line 28) to minimize useless prefetch operations. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the prioritizing of Hum et al. be based on a conditionality of branching, as taught by Taniani et al., for the desirable purpose of minimizing useless prefetch operations (column 3, lines 46-52, column 11, line 35-column 12, line 28).

36. Claim 21 does not recite limitations above the claimed invention set forth in claim 8 and is therefore rejected for the same reasons set forth in the rejection of claim 8 above.

Conclusion

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37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993.

The examiner can normally be reached on Monday-Friday, 8-4:30.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm


RICHARD L. ELLIS
PRIMARY EXAMINER